

## AC TERMINATION

### WHEN TO TERMINATE TRANSMISSION LINES

A transmission line should be terminated if the length of the line, or trace, satisfies the inequality

$$L > \frac{T_r}{2 T_d}$$

L is the length of the transmission line,  $T_r$  is the signal rise time at the source and  $T_d$  is the propagation delay per unit length of the transmission line.

The typical propagation delay for common trace widths and PCB materials is approximately 1.7 nsec per foot. For a rise time of 2 nsec, the critical length determined from the above inequality is:

$$\begin{aligned} L &= \frac{2\text{nsec.}}{2 \times 1.7 \text{ nsec/ft.}} \\ &= 0.59 \text{ ft.} \\ &= 7 \text{ in.} \end{aligned}$$

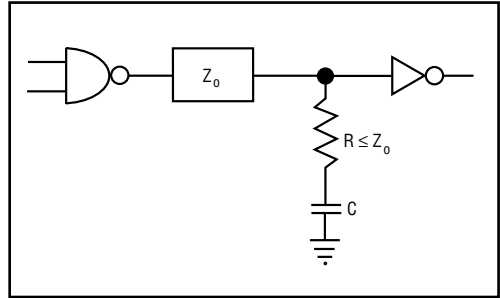
In other words, line lengths greater than or equal to 7 inches should be terminated. Line terminations are needed for clock inputs, read/write strobe lines on SRAM's and chip select and output enable lines on PLD, PROM and RAM devices. Terminations are not needed on address and data lines since they generally operate at lower speeds.

### WHERE TO TERMINATE TRANSMISSION LINES

The termination should be applied at the load which is electrically farthest from the source. This load is usually located at the farthest physical distance from the source.

## PARALLEL AC TERMINATION

The Parallel AC Termination network is a general purpose termination that is preferred over a simple series or parallel termination. An example of the Parallel AC Termination is shown in Figure 1.



**FIGURE 1.** Parallel AC Termination

### WHY AN AC TERMINATION

- Prevents DC power loss since DC current is blocked by a capacitor.
- Does not produce level shift in the output high voltage,  $V_{OH}$ , or output low voltage,  $V_{OL}$ .
- Attenuates high frequency AC noise peaks to levels less than the signal.

### PARALLEL AC TERMINATION'S FUNCTION AS A LOW PASS FILTER

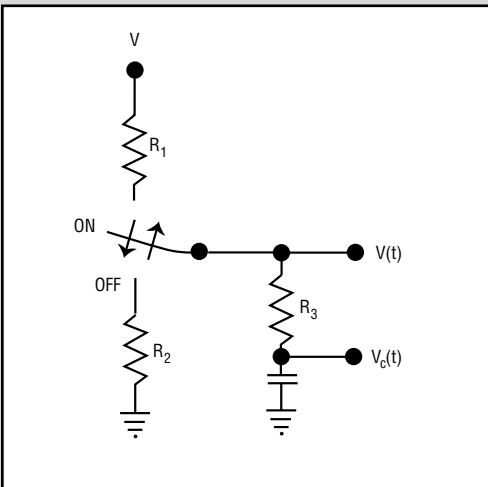
The Parallel AC Termination also serves the secondary role as a low pass filter. This is demonstrated by evaluating the negative and the positive step functions of the circuit shown in Figure 2. To evaluate the negative step function response, the switch in Figure 2 is toggled from the ON position to OFF after the circuit has reached its steady state in the ON position at  $t=0$ . At time  $t=0^+$ , the voltage across the capacitor,  $V_c(t)$  is equal to  $V$ .  $V_c(t)$  is then given by:

$$V_c(t) = V e^{-t/(R_2+R_3)C} \quad (1)$$

In evaluating the positive step function response, the switch in Figure 2 is flipped from the OFF position to ON at  $t=0$ . The voltage across the capacitor  $V_c(t)$  is expressed as:

$$V_c(t) = V[1 - e^{-t/(R1+R3)C}] \quad (2)$$

In theory,  $V_c(t)$  reaches  $V$  in the positive step response when  $t$  equals infinity. In the practical case,  $V_c(t)$  reaches 0.98 of  $V$  after 3.9 time constants,  $RC$ . Likewise, in the negative step response  $V_c(t)$  reaches 0.02 of  $V$  after 3.9 time constants



**FIGURE 2.** AC Termination:  
Low Pass Filter Model

**CALCULATING THE CAPACITANCE OF THE PARALLEL AC TERMINATION**

**The Ideal Case**

The parallel AC Termination is designed with a capacitance,  $C$ , which is large enough to filter positive (rising) and negative (falling) glitches. In addition, it is designed not to be so large as to cause any signal delay beyond the design threshold or to increase signal rise and fall times to be greater than 5 nsec. In short, the value of the capacitance is limited by maximum and minimum values.

For  $R1=0$ , equation (2) becomes:

$$V_c(t) = V[1 - e^{-t/RC}] \quad (3)$$

where  $R = R3$ .

From equation (3) the time,  $T$ , required for the signal to rise from 10% to 90% of the full amplitude is calculated as:

$$T = 2.2RC \quad (4)$$

Solving for capacitance gives:

$$C = \frac{T}{2.2R} \quad (5)$$

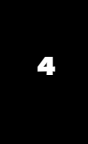
For a line impedance of  $50\Omega$ , the value chosen for  $R$  is  $47\Omega$  since  $R \leq Z_0$  (see Figure 1) and  $47\Omega$  is a standard value. Substituting 5 nsec and  $47\Omega$  into equation (5),

$$C = 48 \text{ pF}$$

Since positive and negative pulses of width  $T$  will be eliminated if  $T < 4RC$ , a glitch of width 9 nsec or less will not be passed by the filter.

**The Real World**

In reality, the values  $R1$  and  $R2$  in Figure 2 need to be taken into consideration. These resistance values are determined from the data sheets of the components connected to the trace or line.  $R1$  is added to  $R3$ , in this case  $47\Omega$ , to find  $R$ . The capacitance,  $C$ , is then calculated from equation (5). The time constant,  $RC$ , must not violate the line's minimum pulse width criteria of the design. Use a smaller  $C$  if the minimum pulse width criteria is violated.  $R2$  is also added to  $R3$ , again  $47\Omega$  in this case, to find  $R$ .  $C$  is again calculated from equation (5). If  $RC$  violates the line's minimum negative pulse width criteria, reduce the capacitance.



### **WHY USE BI TECHNOLOGIES RC NETWORKS FOR AC TERMINATIONS**

- Provide improved reliability over discrete RC networks.
- Real estate savings of 50% compared to discrete components.
- Pick and place cost saving of 50% compared to discrete RC networks.
- Increased board yields due to component count reduction.
- Reduced PCB trace routing problems.
- Minimized PCB trace inductance with RC chips.
- RC chips permit placement very close to active devices.

### **WHICH BI TECHNOLOGIES RC NETWORKS TO USE FOR AC TERMINATIONS**

- Model RC 4
- Model RC 6 circuit types B, C and E