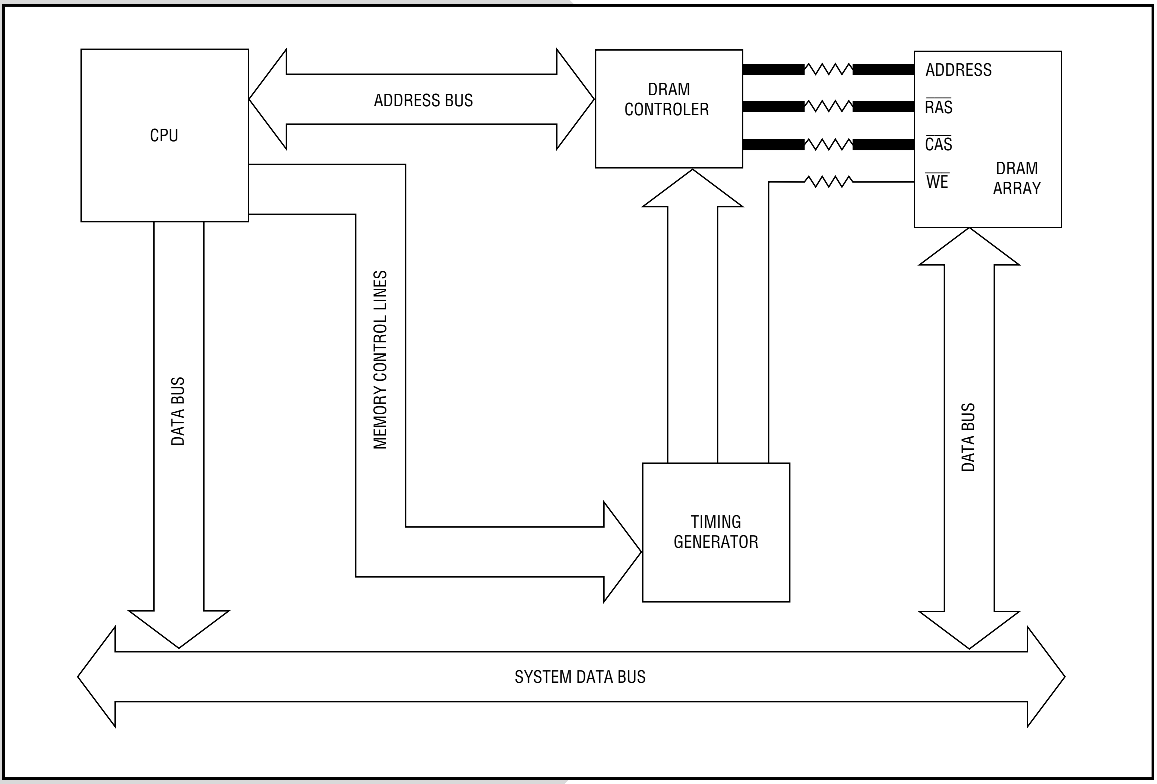
NETWORKS IN DRAM APPLICATIONS

EXAMPLE DIAGRAM OF A DRAM SYSTEM



USE BI RESISTOR NETWORKS TO:

- Match impedance between the memory driver and the DRAM array.
- Minimize reflections and ringing in DRAM inputs.
- Prevent undershoot of RAS, CAS, and WE signals, that could cause latch-up of DRAM inputs.
- Improve system performance by allowing faster settling times for DRAM inputs.

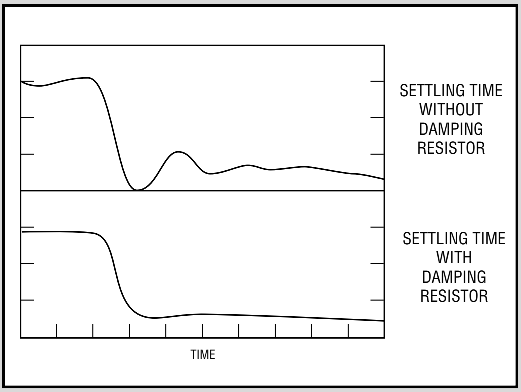
NEED FOR DAMPING

The address lines ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$) and control lines ($\overline{\text{WE}}$) of dynamic RAM arrays are driven in parallel. This causes significant loading on the driver of the DRAM arrays. Each DRAM control input ($\overline{\text{WE}}$) has capacitive loading between 5pF to 7pF, while each address line input has about a 10pF load.

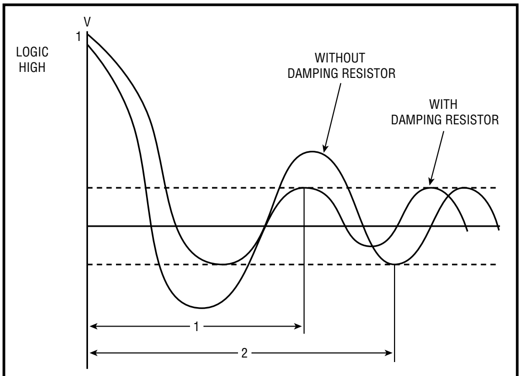
Each DRAM input can therefore be modeled as a transmission line with distributed inductance and capacitance. If not properly terminated, signal reflections and ringing on the line will result, adversely affecting the performance of the memory system. The effects on signal transitions will be:

1. Increased settling time delay on low-to-high transitions.
2. Voltage undershoot on high-to-low transitions.

EFFECT OF DAMPING ON ADDRESS AND CONTROL LINES



Increased settling time due to ringing reduces the system performance because the design has to allow for the settling delay before latching data. Undershoot, by bringing the input voltage below 0 volts, can damage the driver IC as well as alter the DRAM's internal address register contents, causing data errors.



(1) - TIME TO ACCEPTABLE "LOW" LOGIC LEVEL WITH DAMPING RESISTOR
(2) - TIME TO ACCEPTABLE "LOW" LOGIC LEVEL FOR DRIVER WITHOUT DAMPING RESISTOR

APPLICATION GUIDELINES

Termination of address and control lines is typically accomplished with low-valued resistors placed in series at the driver output. Selection of the proper resistance value is performed in two steps:

1. Approximation of the proper resistance using transmission line equations.

2. Breadboarding and changing the resistance value to account for real world deviations such as PCB vias and bends.

The applicable transmission line equations are:

Z_0 = characteristic line impedance (microstrip)

$$= \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right) \text{ohms}$$

T_d = propagation delay of the line

$$= 0.085\sqrt{\varepsilon_r} \text{ ns/in}$$

$$= 1.017\sqrt{0.475e_r + 0.67} \text{ ns/in.}$$

C_0 = trace capacitance = 1000 (T_d/Z_0) pF/in.

C_d = equivalent trace capacitance per DRAM line.

= 7 pF/in.

Z_0' = effective characteristic impedance, including DRAM capacitive loading

$$= \frac{Z_0}{\sqrt{1 + C_d/C_0}}$$

T_d' = effective propagation delay

$$T_d = T_d\sqrt{1 + C_d/C_0}$$

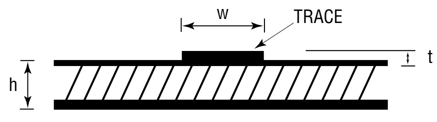
where e_r = relative dielectric constant of the substrate

ε_r

= distance from the trace to the ground plane

w = width of trace

t = thickness of trace



For example, for a trace with the following characteristics:

	ε_r	=	5 (for G10 glass epoxy)
	h	=	0.060 inch
	w	=	0.010 inch
	t	=	0.003 inch
then,	Zo	=	120 ohms
	Td	=	0.19 ns/in.
	Co	=	1.58 pF/in.
	Zo	=	51 ohms
	Td	=	0.44 ns/in.

A theoretical resistance of 51 ohms will match the trace impedance of the PCB.

The necessary resistance will differ from this value due to non-ideal characteristics of the PCB trace geometry (i.e., bends, curves and vias in the trace), as well as the manufacturing variations inherent in the components and materials. A trial-and-error process must be employed in order to optimize the value of the damping resistor.

The procedure involves selecting various values around the calculated value and observing the resulting waveforms on an oscilloscope. Choose the value that best balances the reduction in ringing/reflection and the reduction in speed - a large resistance value provides better damping, but will also add delay by slowing the edge rate. Typically, resistance values for memory damping will be in the range of 10 ohms to 50 ohms, with the most common values in the 20 ohm to 30 ohm range.

Since memory damping is a type of series termination, distributed loading along the line will not be possible. That is, the entire lumped load must be located at the end of the line, with no other loads along the signal path. This will guarantee that the waveform will remain undisturbed as it travels along the line. For related reasons, the placement of the series damping resistor should be as close to the driving device as possible.

BI NETWORKS FOR MEMORY DAMPING

BI can supply a wide range of resistor networks for memory damping applications. Standard resistance values are normally in stock. Any value within the range of 22 ohms to 1 megohm can be supplied.

The following BI Network products make excellent choices for memory damping applications.

- Through hole DIP packages
  898 or 899 Series
- Through hole SIP packages
  BH or BL Series
- Surface mount packages
  Models 627A or 628A small outline DIP
- Model BCN

All models above are available in standard resistance values from 22 ohms to 1 megohm.